REMARKS

Claims 15, 22 and 25 have been amended make clear that the level compensating film (of claim 15), second layer of the upper insulating film (of claim 22) and spin on glass film (of claim 25) is not disposed over the tops (i.e., highest levels) of metal wiring and that the pad metal is over the active element. These amendments overcome the new matter rejection and further distinguish the applied prior art.

Further, claim 22 has been amended to make clear that the trilaminar upper insulating film has an upper (third) layer that covers the metal wiring layer and a second (level compensating) layer that does not cover the tops of the metal wiring layer. The amendment to claim 22 overcomes the concern raised in the paragraph spanning pages 8-9 of the Action.

Claims 28 to 34 have been amended as suggested in the Action. In particular, Claims 32 to 34 have been amended to make more clear that the level compensating film is coplanar with a lower layer of the interlayer insulating film. As this feature is clearly shown in Figure 6, the rejection under the Section 11, para. 1 of claims 32 to 34 has been overcome by amendment.

I. The Application Has A Written Description Of A Level Compensating Film That Does Not Cover The Tops Of A Metal Wiring Layer

The rejection of claims 15, 22, 25, 26 and 29 to 34 as not being supported by the written description of the original application (35 U.S.C. §112, 1st para.) is traversed and has been overcome by amendment. As amended, the rejected claims state that the level compensating film/second layer of the upper insulating film/spin on glass film is not disposed on the highest levels of a metal wiring layer. Figure 6 (an annotated copy is attached) shows a level compensating film (10b) that does not cover the tops of a metal wiring layer (9a). The highest levels of the metal wiring layer, i.e., the tops, are marked on the attached Figure 6. Further, Figure 6 shows the pad metal to be over the active element (3, 4a, 4b) and over the metal wiring and the level compensating film.

The claims as amended require the level compensating film to not cover the top of the metal wiring layer in a region below the metal pad. The claims also require the level compensating film to be "between" the metal wiring layer. Figure 6 shows that the level compensating film (10b) rests between the portions (9a, 9b) of the metal wiring layer. Because the level compensating film does not cover the tops of the metal wiring layer and is between the metal wiring layer as is shown in Figure 6, the written description of the specification does support the rejected claims and the section 112 rejection should be withdrawn.

II. Narui Does Not Anticipate The Claimed Invention

The rejection of claims 14, 15, 22, 25 and 26 as being anticipated by Narui et al (US Patent No. 6,150,689 - Narui) is traversed. There is no anticipation because Narui does not disclose: (i) a pad metal over an active element (claims 14, 15, 22, 25 and 26); (ii) a level compensating film/second layer of the upper insulating film/spin on glass (SOG) film that does not cover the tops of the metal wiring layer (claims 15, 22, 25 and 26), (iii) a level compensating film having a minimum thickness for compensating the level difference of a metal wiring layer under the pad metal (claims 15, 22, 25 and 26), and (iv) removing the level compensating film under a pad metal (claim 14).

A. Narui Does Not Suggest A Minimum Thickness Level Compensating Film Which Does Not Cover The Tops Of A Metal Wiring Layer

The anticipation rejection of claims 15, 22, 25 and 26 should be withdrawn because Narui does not disclose a level compensating film/second layer of the upper insulating film/SOG film that is the "minimum thickness necessary for compensating the level difference of a metal wiring layer" or that does not cover a highest level of the metal wiring layer under a pad metal.

In the claimed invention, the pad metal overlies the stack of interlayer insulating layers and wiring layers. Level compensating/second layer/SOG films are typically formed of mechanically brittle materials. External forces applied to the pad metal can break a conventionally thick SOG film below the pad metal. A thick level compensating/second layer/SOG film or such a film that covers even the tops of a metal

wiring layer is prone to cracking. Cracks in SOG film can induce cracks in the overlying pad metal. The claimed invention protects the overlying pad metal by minimizing the thickness of the level compensating/second layer/SOG film and by ensuring that the film does not cover the tops of the metal wiring layer.

The thin SOG film of the claimed invention is less prone to fracture due to forces applied to the pad metal. Reducing the thickness of the SOG film under the pad metal and not covering the tops of the metal wiring layer reduces the tendency that the film will break due to forces transmitted through the pad metal. In addition, the minimum thickness SOG film still compensates for level differences due to the metal wiring layer.

Narui does not include a level difference compensating film formed to a minimum thickness necessary to compensate for the level difference of a metal wiring layer or that does not cover the tops of a metal wiring layer. The Action identifies as an "interlayer insulating film" of Narui the silicon nitride film (27), SOG film (31) and silicon oxide film (32) (see Narui, col. 14, ln. 62 to col. 15, ln. 5) shown in Figures 54, 55 and 61 of Narui. These films 27, 31 and 32 each extend to a height that is substantially higher than and above the tops of the metal wiring layer (30A, B). These films 27, 31 and 32 cover the metal wiring layer (30A, B). Further, these films in Narui are collectively relatively thick and are not formed to a minimum thickness needed level the layers of the semiconductor device by compensating for the gaps in metal wiring at the metal wiring layer (30 A, B). Accordingly, Narui teaches away from the minimum thickness film that do not cover tops of metal wiring that are recited in claims 15, 22, 25 and 26.

B. Narui Does Not Disclose A Pad Metal

Narui does not disclose a pad metal for an electrode pad covering an underlying active element. The rejected claims recite a pad metal for an electrode pad arranged over an active element, metal wiring layer, interlayer insulating film and barrier metal layer. Forming an electrode pad over an active element efficiently utilizes the semiconductor area under the pad. In the past, the area under an electrode pad had not been used for active elements. Application, page 4. The claims have been amended to require the pad metal to be over the active element.

A pad metal (e.g., 14 in Figure 1of this application) of an electrode pad provides a terminal for an external connection to the semiconductor device. The pad metal provides, for example, a terminal for bonding a wire to the semiconductor device. See Appln. pp. 20, 23, 32 and 45. The independent claims state that the pad metal is for an electrode pad that forms "an external electrical terminal to said semiconductor device".

An objective of Narui is to simplify a manufacturing process by commonly carrying out the step of forming an electrode of an information storage capacitor and forming a metallic interconnection with a peripheral circuit. Narui does not suggest a compact architecture for a semiconductor device having a pad metal and does not address the problem of a cracked level compensating film underneath a pad metal.

The Action improperly states that wiring layer 41B in Narui "a capable to function as a pad metal" Action, p. 8. There is no pad metal disclosed in Narui or any structure that is capable of being the pad metal recited in the rejected claims.

Narui, (at column 11, lines 10-52 and particular at column 11, lines 43-52) describes that on a Y select line YS and interconnections 41A and 41B, an interconnection layer is disposed with an insulating film intervening therebetween, and a passivation film is further formed on the interconnection layer with another insulating film intervening therebetween. This indicates that the interconnection 41B in Narui is merely a part of the interconnections of the peripheral circuit, and thus not constituting an electrode pad which is an external electric terminal.

The internal wiring select line (41B) of the memory circuit shown in Narui (Figs. 54, 55 and 61) is not a pad metal. *See* Narui, col. 16, lns. 19-23 and Fig. 3. Contrary to the Action, wiring layer 41B is disclosed in Narui as:

> **A Y select line YS and second interconnection layers 41A, 41B of the peripheral circuit are, respectively, formed on the silicon oxide film 40 as shown.** The interconnection 41A is electrically connected to the plate electrode 35 via a connection hole 42 made at the insulating films (i.e. the silicon oxide film 40, the SOG film 39 and the silicon oxide film 28) which have been formed on the plate electrode 35 of the capacitor C, by which a plate potential ($v_{dd/2}$: a potential corresponding to a half of an applied voltage V_{dd} from outside of the semiconductor chip) is supplied to the plate electrode 35. **The interconnection 41B is electrically connected to the interconnection 30B via a connection hole 43 made at the insulating films (i.e. the silicon oxide film 40, the SOG film 39, the silicon oxide film 38, the silicon oxide film 32, the SOG film 31 and the silicon nitride film 27) which have been formed over the first interconnection layer 30B of the peripheral circuit.** A tungsten (W) plug 44 is embedded in the inside of the connection hole 42 for connection between the interconnection 41A and the plate electrode 35 and also in the connection hole 43 for connection between the interconnection 41B and the interconnection 30B, respectively. **The Y select line YS and the**

> **interconnections 41A, 41B are each made of a conductor film** whose sheet resistance is smaller than those conductor films for the gate electrode 8A (word line WL) and the gate electrodes 8B, 8C and also for the bit lines BL.sub.1, BL_2 and the interconnections 30A, 30B. For instance, such a conductor film is constituted of a three-layer conductor film wherein a TiN film an Al (aluminum) alloy film containing Si (silicon) and Cu (copper), and a TiN film are built up in this order. [Narui, col. 11, lns. 10-43 (emphasis supplied)]
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> Thereafter, a Y select line YS and second interconnection layers 41A, 41B are formed on the silicon oxide film 40, thereby approximately completing the DRAM shown in FIG. 3. **The Y select line YS and the interconnections 41A, 41B are, respectively, formed simultaneously by depositing a TiN film, an Al alloy film and a TiN film on the silicon oxide film 40 by sputtering, and patterning these films by etching through a photoresist mask.** The Y select line YS and the interconnections 41A, 41B may be formed of a built-up film of a TiN film and a Cu film, respectively. [Narui, col. 16, lns. 19-28 (emphasis supplied)]

The Y select line 41B disclosed in Narui is not a pad metal for an electrode pad nor an external electrical terminal. While the memory device that is the subject of Narui may have an associated electrode pad, it is not the Y select line nor is it described in the patent. There is no anticipation because Narui does not disclose a pad metal for an electrode pad.

C. Narui Does Not Disclose Removing The Level Compensating Film Underneath The Pad Metal, As Is Recited In Claim 14

Claim 14 states that the level compensating film is partially removed below the pad metal. Claim 14 as amended specifically recites that the level difference

compensating film under said pad metal is removed. Removal of the film reduces the thickness of the level compensating film underneath the pad metal.

Claim 14 has been amended to state that the level difference compensating film under the pad metal is substantially completely removed. This feature is described in the application at, for example, page 29, line 11 to page 30, line 23 and is shown in Figure 5.

Narui does not suggest removing the SOG film (31, 39) that is above metal wiring (BL_2, 30A) and below the metal layer (41b). The Narui SOG film is very thick below the lower portions of the metal interconnection (41b) and Y select line YS. Because the Narui SOG film has not been removed from below the metal connections 41b and Y select line, there is no anticipation of claim 14 which requires that "a portion of said level difference compensating film under said pad metal is removed."

III. Obviousness Rejections Of Dependent Claims Should Be Withdrawn

The rejection of dependent claim 16 and 27 as being obvious over Narui in view of Hosomi et al (US Patent No. 5,773,888) is traversed for at least the same reasons stated above with respect to claim 14, on which depend claims 16 and 27.

The passivation film (3) disclosed in Hosomi is applied outside the context of the present invention involving layers over an active element having insulating films, metal wiring layers, and a pad metal. There is no suggestion to combine the Hosomi passivation film with the semiconductor memory structure shown in Narui because Narui does not relate to pad metals or the stresses caused when bonding to pads, and Hosomi et al do not suggest that stresses induced by bonding may be alleviated by a passivation film

that covers a large portion of a pad metal. It would not have been obvious to apply Hosomi et al to modify the semiconductor device disclosed in Narui in order to form the claimed invention.

The rejection of dependent claims 28 to 31 as being obvious over Narui and Ng is traversed. Claims 28 to 31 recite a "through hole" in the interlayer insulating film. The through-hole does not penetrate the level compensation film. Narui does not teach a through hole in an interlayer insulating film that does not penetrate the compensation film.

Ng '039 teaches that an interconnection and a pad metal which are identical in width are connected with each other without interposing an interlayer insulating film therebetween. Narui '689 teaches that a plate electrode 35 is provided between a metal layer where interconnections 30A and 30B are formed and an interconnection 41B (which is regarded as a pad metal in the Action). This indicates that an interlayer insulating film in Narui is between the metal layer where interconnections 30A and 30B are formed and the interconnection 41B, which is ad odds with the lack of an interlayer insulating film in Ng. Furthermore, in Narui, the plate electrode 35 is formed between the metal layer and the interconnection 41B, so that a level difference compensating film is required to cancel out the level difference. In this manner, in Narui, not only is an interlayer insulating film required between the metal layer and the interconnection 41B but also this interlayer insulating film has to include a level difference compensating film.

For this reason, one having ordinary skill in the art would not arrive at claims 28-31 of the present application, from the combination of Narui and Ng.

An interconnection 41B of Narui is connected to an interconnection 30B, 35B via through-hole 43 made at an SOG film 31, 39. In contrast, the present application describes the above-mentioned arrangements (i) and (ii) so that as in Figs. 5-8, 10, and 14-18, as a through-hole for connecting the pad metal with metal wiring layer and a through-hole for connecting the metal wiring layers with each other are formed so as not to penetrate the level difference compensating film.

All claims are in good condition for allowance. If any small matter remains outstanding, the Examiner is requested to telephone applicants' attorney. Prompt reconsideration and allowance of this application would be appreciated.

Respectfully submitted,

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